Remarks

Claims 1-22 are pending. Claim 22 is herein added. Applicants submit the amendment does not add new matter. Support for claim 22 can be found on at least page 5, line 6. No other amendments are made herein.

Applicants respectfully submit claims 1-21 are patentable under 35 U.S.C. 103(a) over Chan (U.S. 6,057,212) in view of Talwar (U.S. 6,300,208). As a first point, Chan and Talwar, alone or in combination, fail to teach or suggest all features of independent claims 1, 13, 16 and 21. More specifically, Chan fails to teach or suggest (forming) a current electrode, semiconductor electrode or region having a resistivity above 0.1 ohm-centimeter *within* a semiconductor layer or substrate. Chan's source/drain regions correspond to the current electrode(s), the semiconductor electrode or the region having a resistivity above 0.1 ohm-centimeter, as stated in claims 1, 13, 16 and 21. However, Chan's source/drain regions are not *within* a semiconductor layer or a substrate.

Independent claim 13 states "forming first and second current electrodes *within* a *substrate*...." Chan's source/drain regions are not formed within any substrate. Instead, they are above the silicon channel region. Chan's substrate is element 310 (silicon substrate) in FIG. 3. Even if one was to make the incorrect argument that all the layers that were formed prior to the bonding process shown in Chan's FIG. 1 were considered the substrate, the source and drain regions are formed above all of these layers. Elements 1', 6, 5, 4 and 3 in FIG. 1 correspond to elements 310, 315, 320, 325 and 335 in FIG. 3. (See the Detailed Description of Chan.) Chan's source/drain regions are formed above layer 335. Thus, Chan fails to teach or suggest forming current electrodes within a substrate as stated in independent claim 13.

Independent claims 1, 16, and 21 state (forming) the electrode(s) or the region having a resistivity above 0.1 ohm-centimeter (are) within a semiconductor layer, which Chan also fails to teach or suggest. Chan's source and drain regions are raised source/drain regions because that are not completely below the gate electrode 301 or the gate oxide. Raised source/drain regions are not formed within a semiconductor layer because they are formed by epitaxial growth of an underlying semiconductor layer. Thus, Chan fails to teach or suggest this feature of independent claims 1, 16 and 21.

Although Talwar teaches forming electrode(s) within a semiconductor substrate, which is also a semiconductor layer, this feature of Talwar can not be used in Chan's structure because it would destroy the functionality of Chan. For Chan's structure to incorporate Talwar's teaching of an electrode within a semiconductor substrate, Chan would have to form an electrode in Chan's semiconductor substrate 310, which would destroy the functionality of Chan because the electrode would not have the electrical properties Chan desires. Chan is forming a transistor on a back plane. (See columns 1 and 2 of Chan.) If Chan forms a transistor, and hence electrode in the semiconductor substrate 310 no back plane will be present and thus the functionality of Chan is destroyed. Thus, at least this teaching of Talwar can not be used in Chan's structure.

For the above reasons, the combination of Chan and Talwar fails to teach or suggest (forming) a current electrode, semiconductor electrode or region having a resistivity above 0.1 ohm-centimeter *within* a semiconductor layer or substrate of the independent claims 1, 13, 16 and 21. For at least the same reasons, the dependent claims are patentable.

As a second point, even if the combination of Talwar and Chan taught or suggested (forming) a current electrode, semiconductor electrode or region having a resistivity above 0.1 ohm-centimeter within a semiconductor layer or substrate, the combination is not proper. In order for Talwar to be combined with Chan as the Examiner submits there must be teaching, suggestion or motivation from the prior art. Applicants submit that neither Talwar nor Chan teach, suggest or motivate a skilled artisan to combine the references as the Examiner combines them.

In FIG. 3, Chan teaches a back gate insulator 325, a silicon channel 335 and transistor with raised source/drains S,D over a metal layer 320. Talwar in col. 7, lines 13-20 teaches using a laser to active his source/drain regions 5, 6. (See Talwar's FIG. 2F.) As shown in FIG. 2F, Talwar's source/drain regions 5,6 are embedded within the semiconductor substrate 2.
The Examiner contends that by applying Talwar's laser anneal process to Chan's FIG. 3, will inherently cause Chan's metal layer 320 to act as an energy absorbing layer, "expose the energy absorbing layer to an energy source to raise a temperature of the energy absorbing layer" and activate the source and drains of Chan by receiving heat from the energy absorbing layer. Applicants contend that there is no motivation to use Talwar's laser anneal on Chan's structure in FIG. 3.

The Examiner contends that motivation for combining Talwar's laser anneal with Chan's structure "as is taught by Talwar et al., is to activate the source/drain regions (col. 7, lines 13-15)." As discussed above, Talwar's source/drain regions 5,6 are within the semiconductor substrate 2 and thus, Talwar needs to activate them. However, there is no teaching or suggestion in Chan that the source/drain regions need to be activated. Furthermore, it can not be assumed that Chan's raised source/drain regions need to be activated as Chan's raised source/drain regions can be formed by epitaxially growing the regions from the underlying silicon channel and doping the regions during growth. As discussed above, raised source/drain region are formed by epitaxial growth. Since Chan and Talwar fail to provide a teaching or motivation for the combination of the teachings as the Examiner combines them in regards to independent claims 1, 13, 16 and 21, all pending claims are patentable over Chan and Talwar for another reason.

In regards to newly added claim 22, Applicants submit that Chan and Talwar fail to teach or suggest an energy absorber layer comprising an electrically insulating material. Both Chan and Talwar teach metal layers for any energy absorbing layers.

Upon reviewing Talwar again, Applicants now realize that they made an error and did not fully appreciate Talwar at the time of responding to the previous Office Action. The statement that Talwar fails to use an energy absorbing layer to activate the source and drain regions as discussed in the previous response to the Office Action is overly broad and therefore, erroneous. See FIG. 2F and columns 7, lines 12-15 of Talwar. Applicants did not appreciate the teaching of FIG. 2F of Talwar at that time because the Examiner only referred to FIGs. 1 and 3 of Talwar in the rejection. Upon reviewing Talwar again, Applicants have reviewed FIG. 2F. Applicants bring this to the attention of the Examiner to comply with 37 C.F.R. 1.56. Regardless, for the reasons in the other paragraphs above, Talwar even in combination with Chan fails to teach or suggest other features of the claims.

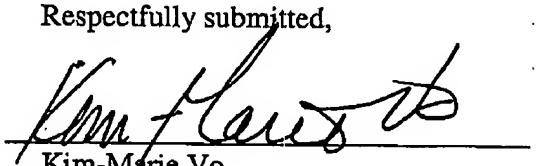
Applicants believe to have responded to all issues presented in the last Office Action. If there are any issues regarding the application, please contact Applicants' practitioner listed below.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Motorola, Inc.
Law Department

Customer Number: 23125

By: 

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